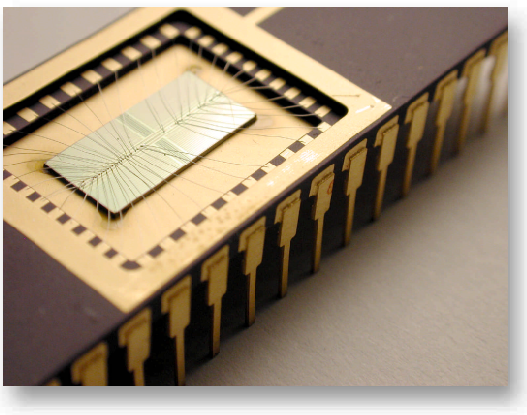
Section 3

MICROELECTRONICS RESEARCH AND EVALUATION ACTIVITIES



Excellence in the selection, evaluation, and acquisition of reliable microelectronics for space applications based on the latest technical knowledge, superior laboratory capabilities, efficient and cost effective processes, and commitment to customer service.

EPE Vision Statement

Radiation Effects

The Radiation Effects Group provides technical guidance and radiation testing for JPL projects relating to space radiation effects on microelectronic and optoelectronic components that are used in JPL projects, as well as projects at other NASA centers. In order to do this task effectively, it is necessary to have a highly trained staff that can respond quickly to project needs and is aware of emerging issues in microelectronic technology and its relationship to radiation vulnerability in space. About 25% of the effort within the group is devoted to applied research on radiation effects in advanced devices, in order to maintain technical awareness.

Radiation testing, modeling and analysis is done to support three different types of effects that occur in space:

- Single-Event Effects, which are caused by the passage of a single energetic cosmic particle or proton, and can produce upsets, latchup or burnout in microelectronics;

- Total Dose Effects, which are the result of ionization from electrons or protons in space, and produce permanent degradation in many types of microelectronic devices; and

- Displacement Damage Effects, which occur when high-energy electrons or protons interact with a lattice atom, permanently changing the lattice characteristics and the properties of microelectronic or photonic devices.

Special analysis methods have been developed to deal with radiation effects in devices, and to calculate the net effect of various environments on microelectronic and optoelectronic devices. An advanced device analysis code is available to determine how charged particles affect microelectronics. This code can provide two-dimensional or three-dimensional analysis.

JPL has internal facilities for total dose testing, including a unique facility for tests at very low dose rate. Single-event testing and displacement damage testing is done at high-energy accelerators, located at universities or government laboratories. The Radiation Effects Group performs about 20 off-site radiation tests annually to support project and research requirements.

Special equipment has been developed for off-site tests, including test fixtures and data collection equipment that is capable of high-speed testing in the vacuum chambers that are required for many of the accelerators, including the capability to vary device temperature over a very wide range. Other equipment is available that allows devices to be mechanically thinned, for irradiation from the back of the package, or removed from the normal package and rebonded in a package that allows irradiation from the top.

Electrical and photonic test equipment is available to characterize permanent damage effects in a variety of devices. This includes special test systems for digital and analog devices, a spectrometer and low-level detection equipment for optoelectronics, and characterization of very large memories.

Advanced Dynamic Memories

Dynamic random access memories (DRAMs) are used in many space systems, particularly in solid-state recorders. As these devices advance in design and complexity, their radiation response becomes more complex. For example, protons and heavy ions would cause single-event upset in older DRAMs, affecting only one cell location. New DRAMs are much more complicated. Single-event upset can alter the overall chip operation if the upset occurs in an internal register that controls memory operation. It is also possible for a single particle to cause numerous cells to upset. A new effect, hard errors, results in permanent stuck bits after a heavy particle or proton strikes a memory location.

In 2002, we investigated hard errors in 64-Mb synchronous DRAMs. One of the important findings was that hard errors are produced in advanced DRAMs by particles with low LET as shown in Figure 3-1, dramatically increasing the number of hard errors that will be produced in space compared to older DRAMs. Note also that the cross section for hard errors increases rapidly as the LET increases.

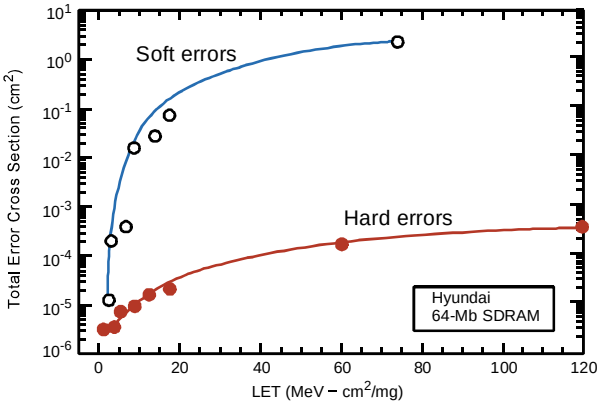


Figure 3-1: SEU test results on 64 Mb SDRAM

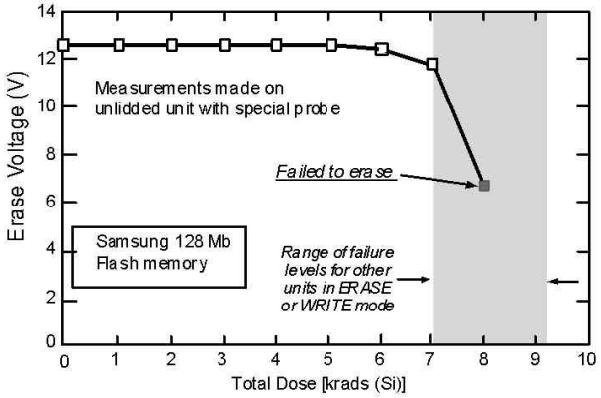


Figure 3-2: Total dose test results on Samsung 128-Mb flash memory

Hard errors are very important in space applications of high-density memories because they limit the effectiveness of error correction methods. Some form of error correction is usually required in order to use high-density DRAMs in space applications.

Additional work was done to investigate and model the dependence of cross sections for single-event upset in advanced DRAMs on LET. This is an important practical issue because the LET dependence and the interpretation of effective LET for ions that strike the device at other than normal incidence affects the upset rate in space. Those results were published in "Modeling the Contribution of Diffusion to Device Upset Cross Section," J. Patterson and L. Edmonds, IEEE Trans. Nucl. Sci., 49(6), pp. 3067-3074.

Non-Volatile Memories

There is a great deal of interest in using non-volatile memories, such as flash memories, in space because they offer extremely high storage densities as well as non-volatile storage. The Radiation Effects Group has investigated flash memories for several years. Those investigations have shown that all flash memories are extremely sensitive to total dose degradation because they use internal charge pumps to generate the 12-20 voltage required to erase and write these types of memories. Figure 3-2 shows test results where the internally generated voltage was measured with a special probe. Total dose damage gradually reduces the voltage produced by the charge pump, eventually falling to the point that it is no longer possible to erase or write to the memory.

For some systems it is possible to add shielding to reduce the total dose on non-volatile memories. A series of tests was done for the X2000 project to show how shielding, in combination with a special sequence of unbiased and biased irradiations, allows flash memories to be used in systems with much higher radiation levels.

Additional work has been done to investigate radiation degradation of emerging flash memories with 512-Mb of storage as well as advanced devices that store multiple logic levels within a single storage element to increase storage density. The latest results are published in "SEE and TID Response of Emerging Non-Volatile Memories," D. Nguyen and L. Scheick, IEEE 2002 Radiation Effects Data Workshop, pp. 62-66.

Microprocessors

A significant amount of work has been done during the last three years to evaluate commercial PowerPC microprocessors. These tests are very complex, requiring special hardware and software to exercise the device during testing and identify errors or malfunctions during irradiation. Special hardware has been developed for this purpose that uses a very simple operating system in order to increase the control and visibility of device operation, and operate at very high speed.

Special packaging is used for commercial processors that uses a "flip chip" ball grid array. It is not possible to get direct access to the top surface of the die with this type of package. The Radiation Effects Group has used special equipment to mechanically reduce the thickness of the back of the package and die, allowing heavy-ion irradiation to be done from the back. This approach has been used for radiation tests of 5 different types of PowerPC microprocessors.

The latest work has compared new silicon-on-insulator devices with feature size below 0.2 mm with earlier generations that were fabricated on bulk (epitaxial) substrates. Figure 3-3 shows how the upset cross section has improved over several generations. This has reduced the upset rate in deep space for microprocessor registers from about 10^{-6} errors per bit day to< 3 x 10^{-8} errors per bit day.

These results were published in a paper entitled "Single-Event Upset in Commercial Silicon-on-Insulator PowerPC Microprocessors," F. Irom et al., IEEE Trans. Nucl. Sci., December, 2002.

Highly Scaled Devices

Extensive work has been done to determine how the rapid advances in commercial CMOS technology will affect radiation hardness, which is of key importance in order to establish how rapidly evolving microelectronic devices can be used in future systems. It is particularly important because there can be numerous changes in commercial technologies in time intervals that are much shorter than the development time for space projects. Several activities are needed for this task:

(1) maintaining an awareness of the practical and physical factors that affect device scaling,

(2) working with commercial manufacturers to determine how their concerns with atmospheric neutron and alpha particle effects have modified device designs, and

(3) doing radiation tests on advanced devices, as they become available, and interpreting their response in a way that is consistent with scaling arguments.

Several papers and presentations have been made on this subject, including an invited paper, "The Effects of Scaling on Radiation Susceptibility," A. Johnston, presented at the 2002 RADECS Workshop. Figure 3- 4, from that paper, shows how the cross section for single-event upset has changed during the last five years for advanced CMOS devices.

Latchup

Latchup from heavy ions and protons continues to be an important practical problem for CMOS devices in space. There have been recent attempts to design special circumvention circuits to detect the high-current condition that results after latchup and quickly remove power to avoid destruction.

Unfortunately, there are many different internal locations within these devices that are sensitive to latch-up. If the high current flows through a narrow metallization region, which is designed for low current (during normal operation), the metallization can actually melt during latch-up. Melting can occur within only a few microseconds, making it nearly impossible to use latch-up circumvention. The microphotograph in Figure 3-5 shows ejected metal spheres from a latch-up event in a CMOS analog-to-digital converter. In this case the void created by the ejected metal created a break in the metallization, but that does not always occur.

These results were published in a paper entitled "Latent Damage in CMOS Devices from Single-Event Latch-up," H. Becker et al., IEEE Trans.

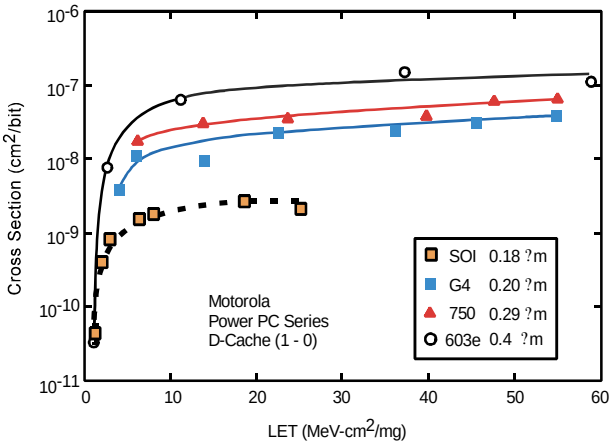


Figure 3-3: SEU test results on the PowerPC microprocessors

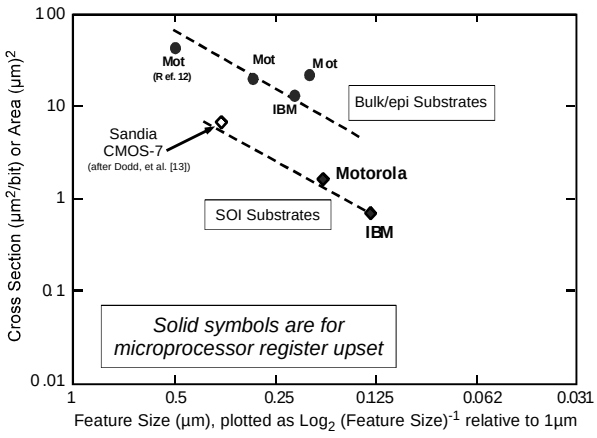


Figure 3-4: Scaling effects on SEU rates for the advanced commercial CMOS technologies

Nucl. Sci., December, 2002. The paper shows examples of latent damage and establishes a threshold current density of 3 x 106 A/cm^2 in order to avoid latent damage effects.

The Radiation Effects Group also did extensive work to investigate catastrophic latchup on a digital signal processor that was used in an instrument designed by JPL. It was not practical to replace the component with an alternative part that was not sensitive to latchup, so a series of tests was done to determine the effectiveness of latchup mitigation for this system. The mitigation approach consisted of (a) a hardware method that detected high-current latchup events, shutting off power within 1 ms and (b) a software method, used to indirectly detect lower current events from error signatures generated by the processor. The results showed that although latchup was not always successfully detected, the mitigation approach reduced the probability of catastrophic damage to acceptable risk levels.

Single-Event Transients in Linear Circuits

High-gain linear circuits produce intermediate-duration transients when sensitive internal regions are struck by a heavy ion or proton. Earlier studies by the Radiation Effects Group demonstrated that power control modules used on the Cassini spacecraft could be triggered into an uncontrolled standby mode because of transients in an internal comparator. Fortunately, the cross section for these events in the Cassini application is relatively small, so that only a handful of these erroneous standby modes have occurred. However, single-event transients remain an important issue for space applications.

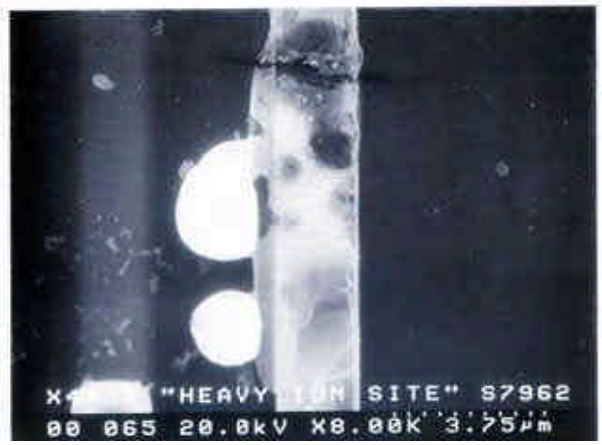


Figure 3-5: The microphotograph of ejected metal spheres from a latch-up event in a CMOS ADC

In 2002, single-event transients (SETs) were investigated in several different types of comparators that have faster response times than the type of comparator used in Cassini. The results in Figure 3-6 showed that the cross section for transients in the high-speed comparators was much lower than for the older LM139 comparator, reducing the number of upsets that occur in space even though the more advanced devices have faster response times.

Extreme Temperature Effects

Most radiation testing is done for applications near room temperature. However, surface exploration missions (such as the Mars Rover) and applications in small spacecraft or on booms may require operation at low temperature. In 2002 a special test fixture was completed that allowed single-event upset measurements to be done at high-energy particle accelerators over a wide temperature range. The lowest temperature that could be achieved with this equipment was approximately 90 K.

Experiments were done on several different types of static memory devices to determine how temperature affected the way that they respond to energetic ions in space.

Micro-electromechanical Systems (MEMS) Devices

Microelectromechanical devices can be susceptible to permanent changes in the electrical voltage required to actuate them. In 2002, total dose effects were investigated on a new type of RF MEMS switch, using GaAs technology. The switches used deposited dielectrics.

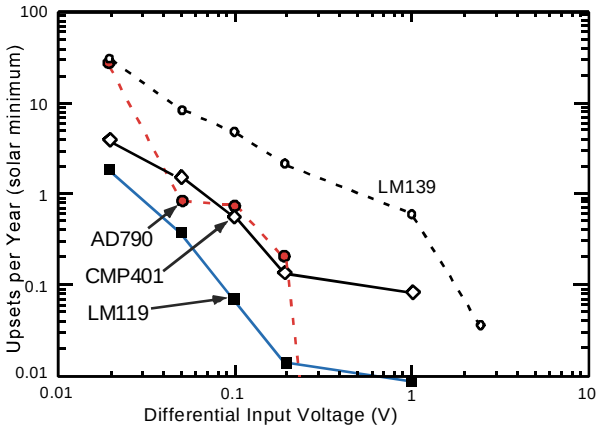


Figure 3-6: SET cross section for high-speed comparators from various manufacturers

Figure 3-7 shows how the actuation voltage changed after the RF switches were irradiated with gamma rays. A technical paper, "Radiation Effects in Microelectromechanical Systems: RF Relays," by S. McClure et al., was published in the IEEE Trans. Nucl. Sci., December, 2002. The paper provides an analysis for the underlying effect, comparing it to older results and models for silicon-based accelerometers.

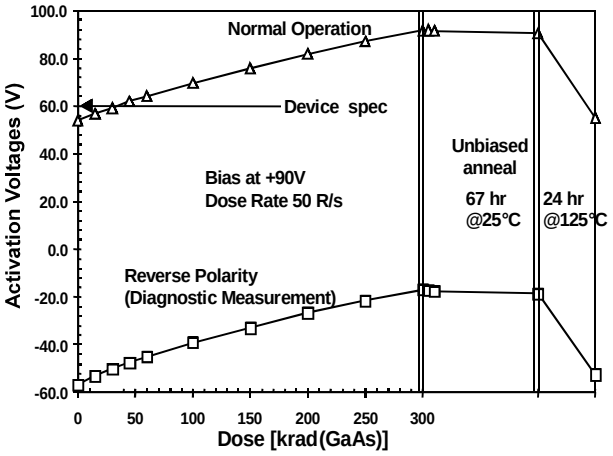


Figure 3-7: RF MEMS switch total dose test and time dependent test results

Reliability and Failure Analysis

The Electronic Parts Engineering Office personnel are constantly investigating various electronic parts technologies for suitability for space applications. Significant investments are made each year in the reliability evaluation of high-payoff technologies with potential for utilization in a space flight system or project. All areas of reliability research provide potential avenues toward finding and enabling particular technologies into space flight systems or subsystems. Furthermore, Office personnel continue to investigate new technologies to improve reliability and performance of space systems. Selected research and evaluation efforts must demonstrate the feasibility of using the commercial technology and advanced technology devices in near-term space applications.

The Office is responsible for performing reliability assessments, characterization, and evaluation of advanced and microelectronic devices including space radiation test and characterization. The work is performed by Office personnel specializing in that branch of research. These highly trained personnel provide strategies to promote technical research, technology evaluation, innovative testing methods and customer education. The following sections provide highlights of the reliability research undertaken in the past year.

Cu-Metallization Reliability

This study addressed reliability issues focusing on Al:Cu and novel Cu interconnects. The work provided a comparison of electromigration failure and failure modes in several different metallization systems, composed of different materials (Al, Cu and Au), different structures, and most importantly, different processes. The work also showed that the Cu metallization in a JPL-sponsored development of micro-inductors would not be able to sustain current densities in standard use conditions.

Failures were identified by a combination of Electron Beam Induced Conductivity (EBIC), Secondary Electron and Rutherford Back-scattering imaging. Failures were due to void formation or metallization shorts through the polymer isolating two metallic layers.

In Al:Cu, subtle differences in electromigration failure due to via/conductor arrangements were examined. Failure modes in Al:Cu conductors were also identified as void formation at the Tungsten plug and Al conductor interface as shown in Figure 3-8. Further work using different shaped vias showed major differences in electromigration behavior due to minor differences in structure geometry. A different shaped via (Tungsten in either conical shape or rod-shaped) has the effect of raising the activation energy for electromigration and delaying both incremental and catastrophic failure in the structures, making the failure times much closer to one another and with a very good fit to a log-normal distribution plot (and hence more predictable). These slight geometrical differences also have an impact on the resistance to greater current densities.

In the work with novel Cu interconnects, collaborations were developed with researchers at the University of Texas in Austin and at International SEMATECH. The Cu interconnects designed by researchers at the University of Texas (at Austin) consisted of four kinds of structures and each structure contained 50 interconnects. Measurements show a clear dependence of void evolution

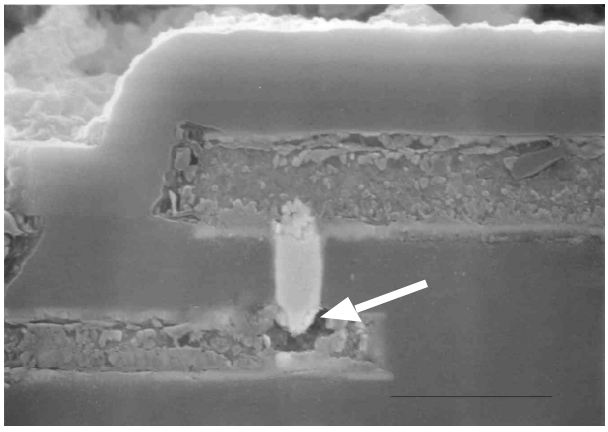


Figure 3-8: Cross-sectional SEM image of voided area at Tungsten/Al:Cu interface. Void was formed from electromigration testing at 240 ℃ and structure failed catastrophically (open circuit).

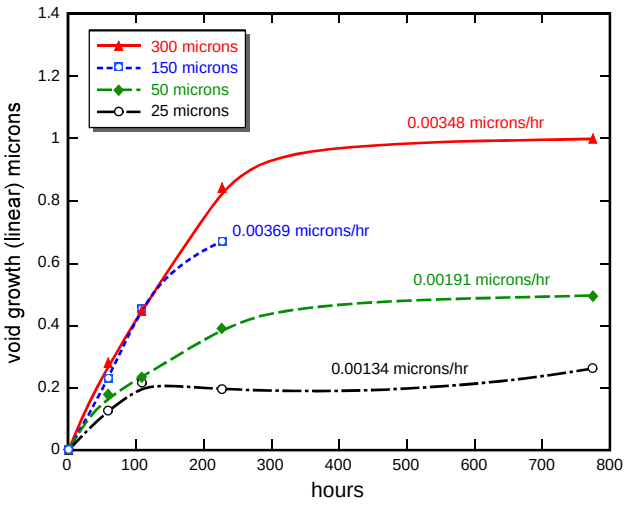


Figure 3-9. Void evolution due to electromigration in Cu conductors of different line lengths

on line length as in Figure 3-9. Void nucleation and evolution was measured for one temperature (240 ℃) and one current density (2 x 106 Amps/cm^2), and this structural data was correlated with the electrical data, which was acquired at regular intervals digitally. The experiment was paused at different time intervals and void evolution was monitored by scanning electron microscopy.

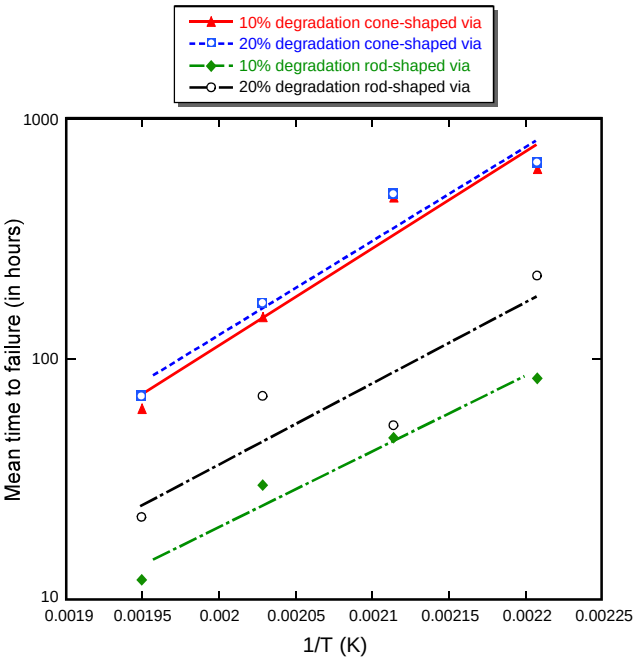


Figure 3-10. Among other differences, the activation energies found for the differently shaped via give 0.62 eV for structures with rod shaped vias and 0.80 eV for cone-shaped vias. This apparently small difference, translates into much different predicted mean time to failure

During electromigration testing of metallization structures of similar materials but different geometries, it was found that the failure modes for catastrophic failure (open circuits) are due to void growth at the Al:Cu cathode and Tungsten via interfaces in all cases. Geometrical differences examined included different conductor/via orientations, and different tungsten via shapes. While the different conductor orientation did not show a statistically significant impact on the metallization reliability, the different via shapes did show an important effect on interconnect reliability. Despite the similarity in failure modes (void formation), differences in activation energy were found to be different by as much as 0.18 eV, and this translates into longer mean times to failure of two orders of magnitude for the most reliable structure as shown in Figure 3-10.

Work summarized in:

R. Leon, D. Vu, A. Johnson, R. Ruiz, J. Okuno, J. Uribe, G. Hather, J.R. Lloyd, " Electrical and Structural investigation of the effects of via-conductor geometry in the electromigration of Al:Cu," presented at the Fall Meeting of the Materials Research Society (2001)

Reliability of RF Devices

This study examined device characteristics as a function of temperature for complementary heterojunction field-effect transistor (CHFET) GaAs devices over a wide temperature range (20 K to 500 K) and presented the variations in device characteristics of isolated and connected GaAs FETs with temperature.

The fully stressed synchronous rectifier CHFET showed some degradation (<10%) after 250-950 hrs of continual stress at 240° C. After 975 hours in fully stressed conditions (up to 4 volts for Vds and Igs 1.75 amperes) the reverse leakage current obtained at -4 V when making two terminal dc measurements increased to 10% of the pre-test value. Preliminary data on life testing for these novel devices was used to estimate mean times to failure for GaAs devices based on 1000 hour testing of their dc characteristics. Calculated mean time to failure (MTTF) was 3.7 x 105 hours (about 42 years), assuming activation energy of 0.7 eV.

Using the equation:

$$MTTF = A \exp [Ea/kT]$$

and using T = 513 kelvins and k = 8.63 x 10^{-5}

we can obtain MTTF = 1.325 x 10^{-4} A exp [Ea /kT]

Therefore, at operating temperatures of 100° C (or 373 K)

MTTF = 3.7 x 105 hours (about 42 years)

Considering that 10% degradation in leakage current is a very stringent definition of failure and that a lower than expected activation energy value was used, this predicted MTTF is quite good.

Work summarized in:

M. Gallegos, R. Leon, D. T. Vu, J. Okuno, S. Johnson, " Accelerated Life Testing and Temperature Dependence of Device Characteristics of GaAs CHFET Devices," presented at the International Integrated Reliability Workshop, Oct 21-24, 2002 in S. Lake Tahoe, CA

Characterization of Quantum Dots for Space Applications

The effects of proton irradiation on quantum dot (QD) carrier dynamics were measured by continuous wave and time-resolved photoluminescence. Results obtained show that the previously demonstrated superior radiation hardness of quantum dots (compared to quantum wells of the same composition) is general across various types of III-V quantum dots. Comparison of irradiation effects on carrier dynamics in thin InGaAs quantum wells to InGaAs/GaAs quantum dot structures with different dot density and substrate orientation, as well as on InAlAs/AlGaAs quantum dots found that carrier lifetimes in QDs are much less affected by proton irradiation than in quantum wells, which can be attributed to the three-dimensional carrier confinement in quantum dots. This research also identified the observed enhancement of the photoluminescence intensity seen in quantum dots after moderate radiation fluences to a more effective carrier transfer from the barrier material into the quantum dots, possibly due to radiation-induced defects providing an additional channel of carrier transfer.

In another set of experiments, spatial ordering of quantum dots by molecular beam epitaxy was achieved. This was accomplished by using misfit dislocations to modify the surface morphology and to attain positional ordering of InAs quantum dots. Misfit dislocations were generated in a strain relaxed InGaAs layer. Influence of quantum dot positional ordering and dot proximity to dislocation arrays on carrier dynamics was studied by time-resolved photoluminescence. Photoluminescence (PL) and time-resolved PL were used to study the effects of increased QD positional ordering, increased QD uniformity, and their proximity to dislocation arrays on their optical properties. These measurements showed narrower inhomogeneous broadening from the ordered quantum dots and differences in the in PL dynamics were found, and are shown in different excitation intensity dependence of the photoluminescence intensity and carrier lifetime, indicating stronger influence of nonradiative recombination for the ordered quantum dot structures.

In another study which included optical and transport measurements carried out on p-n diodes and Schottky barriers containing multilayers of InAlAs quantum dots embedded in AlGaAs barriers, it was shown that while red emission from quantum dot states is obtained at 1.8 eV, defect states dominate the optical and transport properties of these quantum dots. These defect states originate from unintentional impurities (or native defects) introduced during epitaxial growth (not from radiation or processing) and they were fully characterized using deep level transient spectroscopy, among other techniques.

Publication:

R. Leon, J. Ibanez, S. Marcinkevicius, J. Siegert, T. Paskova, B. Monemar, S. Chaparro, C. Navarro, S.R. Johnson, Y.H. Zhang, " Defect states in red-emitting InxAl1-xAs quantum dots," Physical Review B, 66 (8): art. no. 085331 Aug 15 2002

R. Leon, S. Chaparro, S.R. Johnson, C. Navarro, X. Jin, Y.H. Zhang, J. Siegert, S. Marcinkevicius, X.Z. Liao, J. Zou, " Dislocation-induced spatial ordering of InAs quantum dots: Effects on optical properties," Journal of Applied Physics 91 (9): 5826-5830 May 1 2002

Low-k Dielectric Reliability Evaluation

This study evaluated low-dielectric-constant (low-k) materials, which are utilized to replace the interlevel dielectric in integrated circuits. The study also surveyed the materials by type and commercialization potential, to construct a NASA program for under-

standing the materials properties, their behavior in space environments, and the risk to flight projects using such devices. Two classes of materials were identified as suitable targets for further research - silsesquioxanes and organic polyarylenes. Despite their high commercialization potential, chemical vapor deposition (CVD)-materials (SiCOH-type) were found to be unimportant to space applications due to their short production life (~ 5 years, or 1-2 generations of electronics). Under this project, simulation techniques are being developed to better understand the properties of porous low-k materials, which will be introduced as interlevel dielectric materials. Currently, these efforts are unique in the field, thereby offering good leverage for information exchange with industrial partners.

The scaling effects drive the deep sub-micrometer technology devices into high performance and high density integrated circuits (ICs) with tens of millions transistors and multilayer of high-density metal interconnects. The electrical resistance and parasitic capacitance associated with those metal contacts have become a major limitation for the speed of the high-performance devices. This became the fundamental motivating factor for the semiconductor industry to move toward low-k dielectric materials, which reduce the parasitic capacitance between the metal lines. These new materials are used in a new fabrication process to produce the multi-level, high-density metal interconnections needed for advanced high-performance devices. Lately, the trend has moved toward the replacement of silicon dioxide dielectric with new low-k dielectric materials.

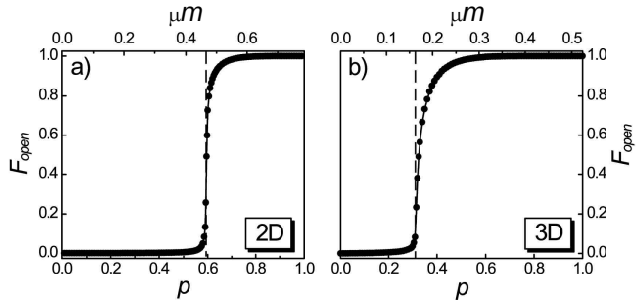


Figure 3-11. Critical percolation in porous media. Open porosity onset: Threshold values taken form the literature

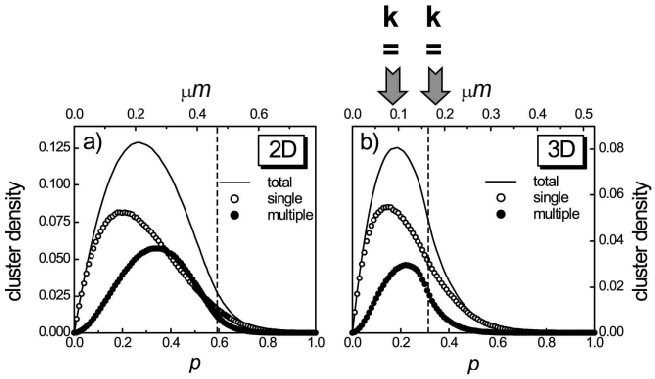


Figure 3-12. Using models to identify critical phenomena

The porous low-k dielectrics combined with copper metallization create a significant integration problem along with reliability concerns. Therefore, a study was conducted to identity reliability issues for the inter-layer dielectric (ILD) materials, and a survey was done to determine which ILD candidates are likely to be used in the next-generation (0.13μm) microelectronic devices. The available data were used to evaluate their performance in hostile space environments.

A survey listing all major low-k materials, selecting research targets, literature survey and identifying reliability issues in space environments was conducted and will need to be updated regularly to reflect the progress in the low-k semiconductor industry. We also studied the currently available low-k dielectric materials to determine the materials most likely to appear in electronic devices in the near future. An experiment was conducted using percolation theory to determine the most likely porosity to be included in these materials We extended percolation theory to predict thermal and mechanical properties of the most relevant porous materials We also evaluated the potential reliability performance of porous low-k dielectric materials based on predicted thermal and mechanical properties, used computational results to leverage information exchange (experiment) with industry and universities, and verified experimentally thermal and mechanical properties of low-k dielectric materials. We established validity of the percolation model through a comparison with the literature, identified relevant porosity parameters and assessed models feasibility as shown in Figure 3-11.

A major difference between k=2.4 and k=2.1 generations was found and is shown in Figure 3-12. The k=2.1 material (porosity: h=17-19%) will contain percolated porosity, which implies significant degradation of mechanical strength, thermal conductivity, compatibility with production steps, etc. The k=2.4 (porosity: h=7-9%) dielectric will contain porosity

with minimum connectivity (maximum isolated clusters).

Publication: "A model for comprehensive studies of porosity in low-k dielectrics", MRS Soc. Symp. Proc., vol. 731, p.W5.20.1 (2002)

Electronics for Extreme Environments

Characterization of the electrical performance of flight and commercial electronic parts under extreme low-temperature environments is critical to understanding the reliability and related failure mechanisms. In addition, the research would identify degradation (primarily Hot Carrier) mechanisms and failure modes affecting reliability of electronics upon exposure at low temperature, and verify if Hot Carrier degradation is a failure mechanism over expected lifetimes of the next generation avionics it enables. Initial measurements of long-term life degradation of power MOSFETs at LN_2 operation are shown in Figure 3-13. Additional measurements are being made to understand this failure mechanism further.

COTS/PEMs Reliability Evaluation

The number of COTS devices used in space applications has been growing during the past several years. This is driven by the new technologies and lower cost of COTS devices. However, it is important to arrive at an understanding of the inherent reliability of COTS devices for space applications.

The main objective of this task was to evaluate COTS PEMs for their inherent quality, reliability, and robustness for use in space applications. This required significant planning and execution to determine what testing was needed, what candidate parts should be selected, and the selection of subcontractor test houses to perform all the required tests and recording of data.

As a result of completing some evaluations and testing, a number of issues and concerns about COTS PEMs has been brought to the forefront. For example, the number of different molding compounds (plastics) on the market is significant. In past years, the glass transition temperature (Tg) of plastic was typically measured above 145° C. Today this number is decreasing to as low as 110° C. There are many published articles that claim that going above the Tg can cause reliability failures in PEM components. This task has made measurements for Tg from different manufacturers as shown in Figure 3-14. As a result of the Tg differences found in PEMs, it is necessary to now include Tg measurements as part of the PEMS qualification and selection process. Additional work is being conducted to better understand many of the reliability issues associated with low Tg PEMs for space applications.

MEMS Characterization

Solid-state RF devices are currently utilized in a wide array of application areas, including satellite communications systems, wireless communications systems, automotive radars, and defense applications. Currently, PIN diode or field effect transistor (FET)-based switches are utilized for their high switching speeds, high-power handling, low drive voltage, low cost, and technology maturity. Reliability and performance assurance characteristics can be drawn from the extensive history of semiconductor reliability research.

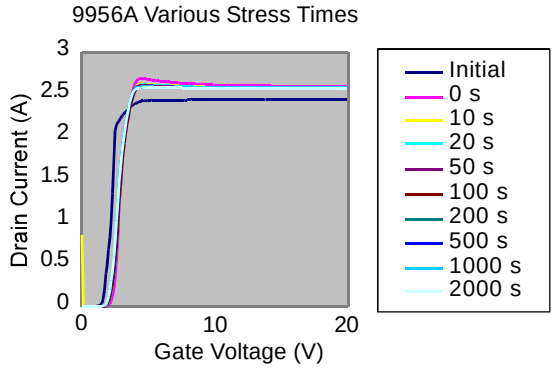


Figure 3-13. LN_2 MOSFET data: Drain current as a function of LN_2 operation over time

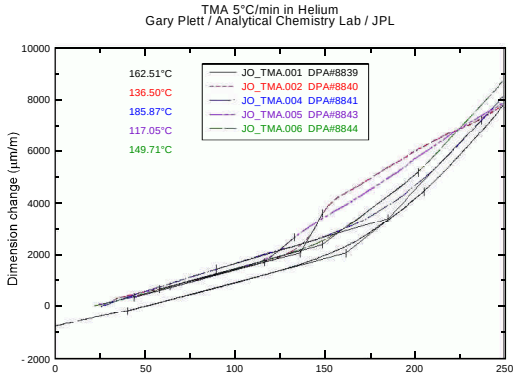


Figure 3-14. Tg measurements for various devices from different manufacturers

The devices of this study were metal-contact switches under ongoing development by the Rockwell Scientific Corporation (RSC). The MEMS switch is a suspended bridge-type mechanical relay fabricated on GaAs substrate, with plasma-enhanced chemical vapor deposition (PECVD) dielectric mechanical structures and Au-based contact metallization. Design and fabrication details are described elsewhere . The transmit-receive (TxRx) devices used in this study were single pole double throw switch devices made up of a configuration of 3 RF MEMS switches in Figure 3-15, one RF MEMS switch in the receive line and two parallel relays in the transmit line to accommodate the higher transmitted power. The relays were activated electrostatically by applying a dc control bias. These TxRx devices were designed, fabricated and packaged by RSC for inclusion in the Micro-Electromechanical-based Picosat-Satellite Inspection (MEPSI) experiment communications board.

MEMS RF technologies offer the advantages of low power consumption (near zero), low insertion loss (~0.1dB up to 40 GHz), and high isolation (>40dB), as well as low volume and low mass. Because of these advantages, RF MEMS has been identified as one of the target technologies that could see high production in the next several years and capture an increased market share. The commercial sector has recognized the potential for large-scale RF MEMS switch production, primarily for telecommunications applications, and the race is on for developing a robust integrated RF MEMS switch design.

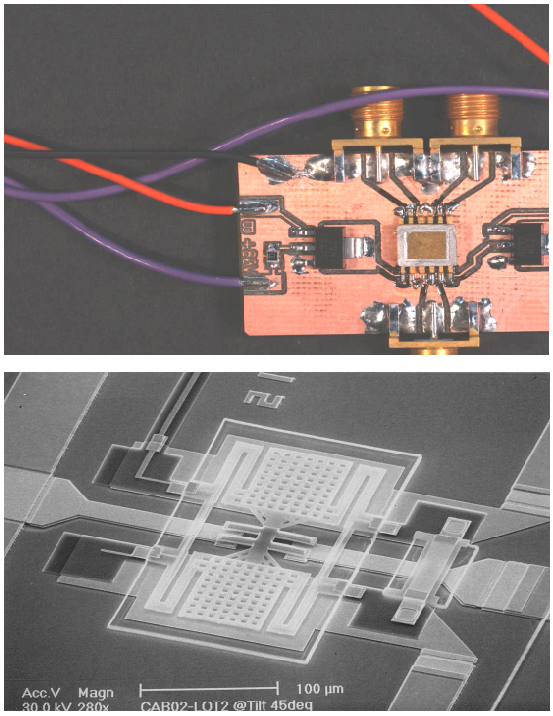


Figure 3-15. MEMS RF switch and test board

The performance advantages outlined above make the infusion of RF MEMS switches (and filters) into NASA spacecraft an exciting leap toward faster, more powerful communications and radiometric systems. For example, currently available commercial RF transceiver solutions are nearing fully integrated on-chip systems, but the switches (and resonators) remain off-chip components. MEMS switches (and MEMS resonators) can help the industry reach fully integrated communications subsystems. In the case of the transceiver, lower insertion loss in the switches between the antenna and the first low-noise amplifier (LNA) leads to lower noise figures and higher sensitivity of the receiver. This effect is magnified when more than one antenna is used, which requires additional switches in the antenna-LNA path. Half-duplex systems utilize RF switches to switch between transmit and receive modes. Redundant systems use RF switches to change between redundant segments. Multiple antenna systems, such as diversity receivers or ping-pong mode radar systems, use RF switches for antenna switching. Virtually all spacecraft with communications or radiometric systems employ such configurations and their performance currently suffers from high insertion loss/low isolation in solid-state RF switches.

Most lifetime testing of RF MEMS devices, up to 500 million cycles, has been carried out at input RF powers of a few mW's . The primary cause of failure in contact MEMS switches is degradation of the contact area metal due to repeated impact between the base and the suspended beam. Pitting, wear, metal migration, and contamination can all contribute to a significant increase in contact resistance and insertion loss. The failure rate is amplified when operating at RF powers over 100 mW because microwelding can bond the pads together, resulting in a permanent short failure. Verification of successful increased power handling broadens the potential application of RF switches in communications systems and makes this work especially relevant for RF MEMS space flight performance assurance.

FPGA Reliability

This work involved a study of high-reliability Field Programmable Gate Arrays (FPGAs) and the methodology of testing devices from two different manufactures: Xilinx and Actel. These two companies use different concepts in designing and manufacturing the devices. Actel uses programmable antifuse (PLICETM) technology and consequently Actel's FPGA are one-time programmable. Xilinx uses a bit-stream (on power up) method and its devices can be programmed multiple times. The reliability issues of high-density FPGAs from these two manufacturers were studied and generated a set of guidelines to mitigate reliability problems and radiation sensitivity through innovative design method.

The FPGA reliability starts with design, which is evolving toward application-specific integrated circuit (ASIC) design methodologies. Life was easy when we were designing and evaluating small-density FPGAs. Nowadays FPGA designers are dealing with over one million gates with very complex logic designs.

One of the major problems faced in designing digital electronic circuits targeted for space is single event upset (SEU) caused by cosmic radiation. Any state-holding digital circuit is susceptible to this phenomenon. In FPGAs, this includes not only the state elements used in the FPGA application circuit (i. e., flip flops and latches), but also the configuration memory, which determines what digital circuit is implemented in the FPGA.

When a ray of cosmic radiation approaches semiconductor material, its energy can excite the semiconductor electrons from the valence band to the conduction band. When this happens, an electron-hole pair is created, resulting in current flow in a transistor channel. In extreme cases, this current flow can be great enough to cause a state-holding cross-coupled inverter or cross-coupled AND gate followed by a NOT (NAND) gate structure to invert its state, from one to zero or zero to one. This is known as a single-event upset (SEU) and can cause a system fault. A related phenomenon is when this current is generated in a parasitic bipolar junction transistor embedded in a CMOS die. Ordinarily, all of the p-n junctions in these parasitic transistors remain reversed-biased, but the radiation-induced current can cause them to become forward-biased. Furthermore, if two such transistors are connected in a positive feedback configuration, they can reach a stable state in which both are forward-biased. This is known as a single-event latchup (SEL).
A reliable system designed for space application must be tolerant of such faults. A common method of achieving such robustness is to use triple modular redundancy (TMR). Triple modular redundancy is a fault tolerance scheme in which a logic subsection, be it a programmable logic arrays (PLA) or a state machine, is replicated three times. The same input is applied to all three modules. A majority gate circuit is then applied to the output to produce the final output of the system. As long as at least two of the modules remain fault-free, the overall system remains fault-free.

An alternative method for achieving system robustness is to check for corruptions in the FPGA configuration memory, and to reconfigure the FPGA if a corruption is detected. This protects against faults in the configuration memory, which can have more serious consequences than faults in the application circuit. Such a scheme was utilized using a Xilinx Virtex-E FPGA. A board was designed in which an FPGA checks its own configuration and forces a reconfiguration if an error is detected. Along with the circuitry for checking its own configuration, an application circuit is programmed into the FPGA in order to demonstrate that such an approach can be used in a normal application. Figure 3-16 shows a block diagram of the overall design. Figure 3-17 shows the flow chart for the readback scheme used in this project.

The main objective of this work was to design a latchup protection scheme. The main limitation to the configuration readback and verification system is that it is only applicable to FPGA-based designs. ASICs and complex programmable logic device (CPLDs) do not have SRAM-based configuration memories, so the procedure is not applicable. A second drawback to this approach is that during the reconfiguration process, the FPGA circuit is not operational. This, too, may represent an insurmountable design restriction. Furthermore, even if it is acceptable for the FPGA to not be functioning, an innocuous configuration memory corruption may result in unnecessary reconfiguration. Generally, not all of the gates available in an FPGA are used in an application.

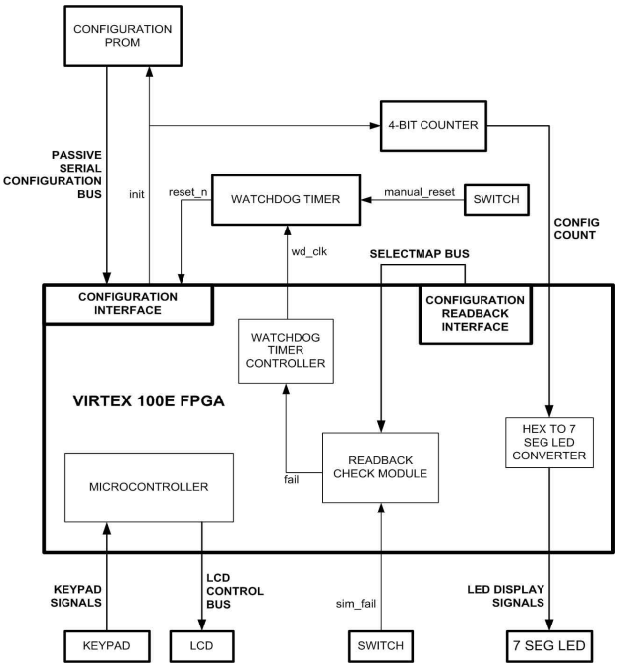


Figure 3-16. FPGA Board Dataflow

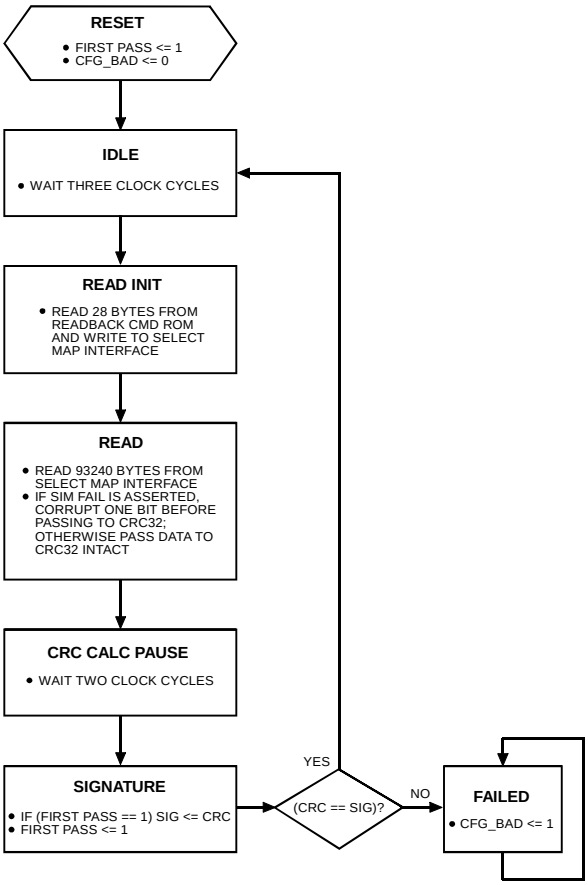


Figure 3-17. FPGA readback check flowchart

There may be instances where a corruption in a portion of the configuration memory (which controls an unused FPGA setting that would not otherwise hinder the performance of the application circuit) results in a reconfiguration.

Both triple modular redundancy (TMR) and FPGA configuration readback and verification add fault tolerance to space-based digital circuits, but both methods have drawbacks. It should be noted that these two methods are not mutually exclusive. The correct choice for which method to use must be made on a case by case basis.

System-on-a-Chip (SoC) Reliability

The ultimate goal of qualification testing for SoC devices is to screen out bad devices from good devices. Eventually it comes down to quality. Therefore, the better the design and qualification tests, the less likely it is that a defective part will survive the test process and be sold to the end user. However, most manufacturers did not incorporate design-for-test (DFT) features into their devices nor did they perform full qualification testing, which presented a challenge for reliability evaluation by the end user.

The cost of qualification testing for very complex SoCs with tens of million logic arrays and embedded memories can be very expensive, especially for those devices fabricated using 0.1-μm process technologies. There are many different factors that affect the cost of testing process such as debugging, time to first tested sample, design for test implementation time, and so on. This task generated evaluation test procedures which addressed a few significant changes in the design and qualification flow to ensure device reliability under reasonable costs.

This method (phased qualification) requires that the design and verification quality is measured and recorded as the design cycle progresses rather than the traditional approach of 'qualifying' by 'reliability tests' a completed 'black-box' design. In this context, qualified means "ready to proceed to the next design phase." The advantages include (1) more visibility provided to the design quality early in the design cycle, (2) the success criteria established in advance rather than after the fact, (3) increased customer understanding and confidence in SoC technology.